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# IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: M. Riedel *et al.*  
Serial No.: 10/728,570  
Filed: December 5, 2003  
Customer No.: 33123  
For: **SYNTHESIS OF CYCLIC  
COMBINATIONAL CIRCUITS**  
Art Unit: 2819  
Examiner: Unknown

## CERTIFICATE OF MAILING PURSUANT TO 37 CFR 1.8

I hereby certify that this correspondence and the attached papers are being deposited with the United States Postal Service with sufficient postage as first class mail on the date indicated below in an envelope addressed to:

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450, on

7-30-04  
Date

Michelle Melendy  
Signature

## INFORMATION DISCLOSURE STATEMENT IN ACCORDANCE WITH 37 C.F.R. §§ 1.97-1.98

Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450

Sir:

Because this Information Disclosure Statement is filed prior to receipt of a First Office Action on the merits of the above-captioned application, a fee for filing this statement should not be due. If, however, it is determined that a fee is due, then any fees that may be due in connection with filing this paper may be charged to Deposit Account No. 50-1213.

In accordance with the duty of disclosure imposed by 37 C.F.R. § 1.56 to inform the Patent Office of all material references known by Applicant or Applicants' representative, this Information Disclosure Statement prepared in accordance with 37 C.F.R. §§ 1.97-1.98 is hereby submitted. The Form PTO-1449 (3 pages) is provided herewith for filing in connection with the above cited application. The cited references that comprise issued U.S. patents are not attached, per the Notice of waiver published in the Official Gazette on August 5, 2003. A copy of the non-patent documents are provided, per 37 C.F.R. § 1.98(a)(2).

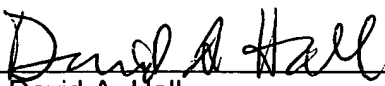
The documents listed on the attached Form PTO-1449 are in the English language. All documents cited in a communication from a foreign patent office in connection with a counterpart foreign application were cited not more than three

months prior to the filing of the attached Supplemental Information Disclosure Statement. A copy of the communication, International Search Report for International PCT Application PCT/US03/38622 (Item D), is also provided. Hence, in accordance with the requirements of 37 C.F.R. § 1.98, as amended effective March 16, 1992, no further explanation of the listed items is necessary.

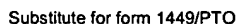
Although these documents and information are made known to the Patent and Trademark Office in compliance with Applicants' duty of disclosure, such disclosure is not to be construed as an admission by Applicants or Applicants' representative that any of the references, singly or in any combination thereof, is effective as prior art against the subject application. In accordance with 37 C.F.R. § 1.97(h), the filing of this Information Disclosure Statement shall not be construed to mean that a search has been made or that no other material information as defined in 37 C.F.R. § 1.56(b) exists.

Applicants respectfully request that the Examiner review the foregoing references and request that they be made of record in the file history of the above-captioned application.

Respectfully submitted,  
HELLER, EHRMAN, WHITE & McAULIFFE LLP

By:   
David A. Hall  
Registration No. 32,233

Atty Docket No.: 18021-6226  
Address all correspondence to:  
**David A. Hall**  
HELLER EHRMAN WHITE & McAULIFFE LLP  
4350 La Jolla Village Dr., 7th Floor  
San Diego, CA 92122-1246  
Telephone: (858) 450-8400  
Facsimile: (858) 450-8499  
EMAIL: dhall@hewm.com



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**Complete if Known**

Application Number	10/728,570
Filing Date	December 5, 2003
First Named Inventor	M. Riedel
Art Unit	2819
Examiner Name	Not yet assigned
Attorney Docket Number	18021-6226

## U. S. PATENT DOCUMENTS

[illegible]

**FOREIGN PATENT DOCUMENTS**

[illegible]

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Substitute for form 1449/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(Use as many sheets as necessary)</i>		Complete if Known	
		Application Number	10/728,570
		Filing Date	December 5, 2003
		First Named Inventor	M. Riedel
		Art Unit	2819
		Examiner Name	Not yet assigned
		Attorney Docket Number	18021-6226
Sheet	2	of	3

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	D	International Search Report for International PCT Application PCT/US03/38622 dated May 4, 2004.	
	E	Robert Allen Short, "A Theory of Relations Between Sequential and Combinational Realizations of Switching Functions", February 1961, pp. 1-115.	
	F	William H. Kautz, "The Necessity of Closed Circuit Loops in Minimal Combinational Circuits", IEEE Transactions on Computers, February 1970, pp. 162-164.	
	G	David A. Huffman, "Combinational Circuits with Feedback", pp. 27-55.	
	H	Ronald L. Rivest, "The Necessity of Feedback in Minimal Monotone Combinational Circuits", IEEE Transactions on Computers, June 1977, pp. 606-607.	
	I	Leon Stok, "False Loops through Resource Sharing", IEEE, 1992, pp. 345-348.	
	J	Sharad Malik, "Analysis of Cyclic Combinational Circuits", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 13, No. 7, July 1994, pp. 950-95	
	K	Anand Raghunathan et al., "Test Generation for Cyclic Combinational Circuits", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 14, No. 11,	
	L	Arvind Srinivasan et al., "Practical Analysis of Cyclic Combinational Circuits", IEEE Custom Integrated Circuits Conference, 1996, pp. 381-384.	
	M	Thomas Robert Shiple et al., "Formal Analysis of Synchronous Circuits", pp. 1-202.	

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	N	Thomas R. Shiple et al., "Analysis of Combinational Cycles in Sequential Circuits", IEEE International Symposium on Circuits and Systems, Vol. 4, 1996, pp. 592-595.	
	O	Thomas R. Shiple et al., "Constructive Analysis of Cyclic Circuits", Paris, March 1996, pp. 1-6.	
	P	Robert de Simone, "Note: A Small Hardware Bus Arbiter Specification Leading Naturally to Correct Cyclec Description", March 1996, pp. 1-8.	
	Q	Amar Bouali et al., "Verifying Synchronous Reactive Systems Programmed in ESTEREL", pp. 1-4.	
	R	Stephen A. Edwards, "Making Cyclic Circuits Acyclic", pp. 159-162.	
	S	R. K. Brayton et al., "Multilevel Log Synthesis", Proceedings of the IEEE, Vol. 78, No. 2, February 1990, pp. 264-300.	
	T	Randal E. Bryant, "Boolean Analysis of MOS Circuits", IEEE Trans. Computer-Aided Design, February 1987, pp. 1-32.	

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